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UNDER TIMING AND SYNCHRONIZATION
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2009 J. A. Abraham HLS 1 High Level
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High-level synthesis raises the design
abstraction level and allows rapid gener-
ation of optimized RTL hardware for
performance, area, and power require-
ments., PDF | Hardware synthesis is a
general term used to refer to the processes
involved in automatically generating a
hardware design from its specification.

High-level synthesis (HLS) could be defined
as the translation from a behavioral
description of the intended hardware
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I might well choose L ..., High-Level
Synthesis 7 Zebo Peng, IDA, LiTH The Basic
Issues • Scheduling Assignment of each
operation to a time slot corresponding to a
clock cycle or time inter-val. • Resource
Allocation Selection of the types of hardware
components and the number for each type to
be included in the final implementation.,
High-level synthesis (HLS), sometimes
referred to as C synthesis, electronic
system-level (ESL) synthesis, algorithmic
synthesis, or behavioral synthesis, is an
automated design process that interprets an
algorithmic description of a desired behavior
and creates digital hardware that implements
that behavior., High-Level Synthesis of

considerations. However, current design methodologies for microfluidic biochips are typically full-custom and bottom up in nature.

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